REMARKS

Claims 1-12 remain in the application. Claims 1-12 stand rejected. Claim 4 has been amended.

In paragraph 5 of the Office Action, the Examiner required an abstract on a separate sheet of drawings. The abstract, which was part of the original PCT application and found at section 57 of that application has been reproduced on a separate sheet as required by the Examiner.

In paragraph 6 of the Office Action, the Examiner objects to citation of certain literature references in that they "may be improper because they appear essential to the claimed invention, especially claim 4." Applicants respectfully request reconsideration of this objection. It's not clear why citing an authority for an assertion is an incorporation by reference of anything. The Examiner has made no showing of why those references contain anything that is essential to the claimed invention. The Examiner has not identified any claim limitation to which those articles could be considered "essential."

In paragraph 7 of the Office Action, the Examiner objected to the use of footnotes in the specification. The Examiner is correct, the specification has been amended to incorporate the footnoted material at the appropriate location in the specification text.

In paragraphs 8 and 9 of the Office Action, the Examiner objects to certain informalities in the language of claim 4 and rejects claim 4 as indefinite for certain informalities of language. All but two of these have been corrected. In line 4 of paragraph 9, the Examiner states that there is insufficient antecedent basis for the limitation of "then 6." Applicant was unable to identify that language in claim 4 and is unable to respond to the rejection. Similarly, in the fourth paragraph of section 9 of the Examiner's action, applicants are unable to find a "reference to the content of 'Figure 14'." Accordingly, applicant is unable to respond to this rejection.

The Examiner rejected claims 1-3 and 5-12 under 35 U.S.C. § 102(e) as anticipated by Turrini and further rejected claims 1-3 and 5-12 under 35 U.S.C. § 102(b) as anticipated by Jain et al.

The Turrini reference is inapplicable to the claims of this application because the entire purpose of Turrini is to do an optimal physical arrangement of the layout of components on a semi-conductor die. Each of claims 1-3 and 5-12 refer to representing the logic of a logic circuit in a vector space. Turrini does not represent the logic of a logical circuit as vectors. Turrini represents an arrangement of components as vectors and then rearranges those components so as to maintain to minimize lead length. However, there is no reduction in the number of components needed in the Turrini patent which would indicate a simplification of the logic.

The claims under rejection also require using the points and vector in a vector space "to simplify the logic of the logical circuit to a simpler form." Turrini does not change the logic of a logic circuit whatsoever. Turrini is used to arrange a set of components so as to minimize lead length. There is no reduction in the number of components in the set.

Thus Turrini does not anticipate any of the rejected claims.

Turning to the Examiner's rejection under of claims 1-3 and 5-12, 35 U.S.C. § 102 as anticipated by Jain et al., Jain et al. do not represent "the logic of a logical circuit" in a vector space.

Jain et al. disclose five embodiments. The first embodiment is directed to a "computer-aided design system and method therefor for performing logic design analysis for determining logical interdependencies between points in a digital circuit topology." See column 3, lines 40-43. Figure 4 is an example of such a topology.

Central to each of the Jain et al. embodiments is the concept of a "cut set". Column 3, line 50 et. seq. discusses a cut set. It states:

> "A cut set in the topology is selected comprising the logic gates falling in a fan-in of the logic gates leading to a target one of the logic gates. A decision diagram is

> built for logic gates in the cut set leading from the target logic gates…. Justification vectors are extracted from the decision diagram for a predetermined Boolean value of the target logic gate."

Figure 6A and 6B illustrate binary decision diagrams (BDDs) and justification vectors for the logic gates shown in Figure 4.

For example, in Figure 6C, the numbers 45 and 46 in circles represent the states of the upper and lower inputs to gate 38 shown in Figure 4. In order for the output of gate 38 to be a logical 1 shown in a rectangle, it is necessary that the state of lines 45 and 46 be both logic zero. However, if both the inputs 45 and 46 are in state logic 1, the output of gate 38 will be logic zero. Thus the binary decision diagram shown in Figure 6C is represented internally in Jain et al. as justification vectors shown to the right hand side of Figure 6C. See column 11, lines 16-30.

It is thus apparent that the justification vectors utilized in Jain et al. do not represent "the logic of a logic circuit" and the justification vectors are not utilized to "simplify the logic of the logical circuit to a simpler form." Thus, Jain et al. do not anticipate the claims of this application.

The second embodiment of Jain et al. relates to logic design verification and not simplification. The third embodiment of Jain et al. relates to logic design verification

using decision diagram simplification. The fourth embodiment relates to decreasing computational resource requirements for constructing a representation of the hardware design. The fifth embodiment of Jain et al. is directed to computer aided design system and method for performing goal directed learning. None of these embodiments in Jain et al. do what is required by the claims of the above-identified application. Accordingly, Jain et al. do not anticipate the claims under rejection.

Accordingly, applicants respectfully request that the Examiner reconsider the rejections of the claims of this application as anticipated by Jain et al. or Turrini.

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Respectfully submitted,

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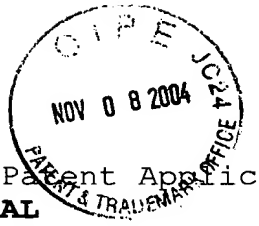

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